D16 Microprogram ROM Bit Functions.

ROM	BIT	NAME	FUNCTION
0	7	BASE/ EXECUTE	Base/Execute enable. When this bit is cleared, the next microprogram cycle will execute out of base address 0; the Base sequence. When set, the next cycle will execute out of the base address specified by IR (Instruction Register) bits 7 through 0; the instruction Execute sequence.
	6	JA6	JA6 through JA0 specify a microprogram jump address within the sequence. If no jump is enabled, this address is ignored and the microprogram counter will be incremented to the next step in the sequence.
	5	JA5	
	4	JA4	
	3	JA3	
	2	JA2	
	1	JA1	
	0	JA0	
1	7	JMP7	Microprogram Jump Enable 7. If set, will execute a jump to the microprogram statement address specified by JA6 through JA0 if IE_INT (interrupts enabled with an interrupt pending) is set.
	6	JMP6	Jump Enable 6. If set, will jump if OVF (Overflow Flag) is set.
	5	JMP5	Jump Enable 5. If set, will jump if CF (Carry Flag) is set.
	4	JMP4	Jump Enable 4. If set, will jump if ID (Indirect, IR bit 10) is set during a Base cycle, or if P (Positive, inversion of Accumulator bit 15) is set during an Execute cycle.
	3	JMP3	Jump Enable 3. If set, will jump if M (Memory Reference, IR bit 8) is set during a Base cycle, or if AC=0 is set during an Execute cycle.
	2	JMP2	Jump Enable 2. If set, will jump if SKIP bit is set during a Base cycle, or if OR=0 is set during an Execute cycle.
	1	JMP1	Jump Enable 1. If set, will jump if /RUN bit is set during a Base cycle, or if IM (Immediate, IR bit 9) is set during an Execute cycle.
	0	JMP0	Jump Enable 0. If set, will jump unconditionally.

ROM	BIT	NAME	FUNCTION
2	7 6	STATE_1 STATE_0	Processor State bits, for application to the Front Panel display. Processor state is indicated as follows, where STATE_1 is the most significant bit: 00, Fetch; 01, Indirect; 10, Execute; and 11, Interrupt.
	5	/IR_LD	If cleared, loads IR from the IDB (Internal Data Bus) at end of cycle.
	4	RUN_CLR	If set, sets /RUN (that is, it clears RUN) at end of cycle.
	3	SKIP_SET	If set, sets SKIP bit at end of cycle.
	2	SKIP_CLR	If set, clears SKIP bit at end of cycle.
	1	IE_SET	If set, sets IE (Interrupt Enable) bit at end of cycle.
	0	IE_CLR	If set, clears IE bit at end of cycle.
3	7	CF_SET	If set, sets CF at end of cycle.
	6	CF_AC0	If set, loads CF with AC (Accumulator) bit 0 at end of. cycle.
	5	CF_AC15	If set, loads CF with AC bit 15 at end of cycle.
	4	CF_CY	If set, loads CF with the ALU (Arithmetic/Logic Unit) Carry output at end of cycle.
	3	CF_CLR	If set, clears CF at end of cycle.
	2	FR_LD	If set, loads FR (Flag Register) from IDB at end of cycle.
	1	/FR_EN	If cleared, enables FR onto IDB.
	0	ALU_OV_EN	If set, loads OV (Overflow Flag) with the ALU two's-complement Overflow output at end of cycle.

ROM	BIT	NAME	FUNCTION
4	7 6 5	ALU_FS2 ALU_FS1 ALU_FS0	ALU Function Select bits. Determine ALU function as follows: 000, Clear; 001, OR minus AC; 010, AC minus OR; 011, AC plus OR; 100, AC xor OR; 101, AC or OR; 110, AC and OR; 111, Set.
	4	ALU_CY_EN	ALU Carry In Enable. If set, CF is applied to the carry input of the ALU. If cleared, 0 is applied (no carry in).
	3	/ALU_EN	If cleared, enables ALU output onto IDB.
	2	PC_INC	If set, increments PC (Program Counter) at end of cycle.
	1	PC_LD	If set, loads PC from IDB at end of cycle.
	0	PC_EN	If set, enables PC onto IDB.
5	7	SP_INC	If set, increments SP (Stack Pointer) at end of cycle.
	6	SP_DEC	If set, decrements SP at end of cycle.
	5	/SP_LD	If cleared, loads SP from IDB at end of cycle.
	4	/SP_EN	If cleared, enables SP onto IDB.
	3	OR_INC	If set, increments OR (Operand Register) at end of cycle.
	2	OR_DEC	If set, decrements OR at end of cycle.
	1	OR_LD	If set, loads OR from IDB at end of cycle.
	0	/OR_EN	If cleared, enables OR onto IDB.

ROM	BIT	NAME	FUNCTION
6	7	ROR	If set, AC executes a rotate right through CF at end of cycle.
	6	ASR	If set, AC executes arithmetic shift right at end of cycle.
	5	LSR	If set, AC executes logical shift right at end of cycle.
	4	SHL	If set, AC executes shift left at end of cycle.
	3	ROL	If set, AC executes rotate left through CF at end of cycle.
	2	AC_LD	If set, loads AC from IDB at end of cycle.
	1	/AC_EN	If cleared, enables AC onto IDB.
	0	SR_EN	If set, enables SR (the Switch Register, on the Front Panel) onto IDB.
7	7	AR_LD	If set, loads AR (Address Register) from IDB.
	6	HI_Z	Bus drive control. If set, the External Buses (External Control Bus, External Address Bus, and External Data Bus) will assume a high-impedance state, and may be used by devices external to the processor.
	5	-SPARE-	Spare bit, unused.
	4	MEM_REQ	Memory Request. When set, asserts /MEM_REQ on ECB (External Control Bus).
	3	IO_REQ	I/O Request. When set, asserts /IO_REQ on ECB.
	2	READ	Read Request. When set, asserts /READ on ECB and enables the EDB (External Data Bus) onto IDB.
	1	WRITE	Write Request. When set, asserts /WRITE on ECB.
	0	INT_ACK	Interrupt Acknowledge. When set, asserts /INT_ACK on ECB.

ROM	BIT	NAME	FUNCTION
8	7	/IX_LD	If cleared, loads IX from IDB at end of cycle.
	6	/IX_EN	If cleared, enables IX onto IDB.
	5	/IY_LD	If cleared, loads IY from IDB at end of cycle.
	4	/IY_EN	If cleared, enables IY onto IDB
	3	-SPARE-	Spare bit, unused.
	2	-SPARE-	Spare bit, unused.
	1	-SPARE-	Spare bit, unused.
	0	-SPARE-	Spare bit, unused.